IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants(s):	Devine et al.
Case:	2-2
Serial No.:	10/787,376
Filing Date:	February 26, 2004
Examiner:	2182
Group:	Jasjit S. Vidwan

Title: Controller for Peripheral Communications with Processing Capacity for Peripheral Functions

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated February 17, 2010, of claims 4, 5, 10, 11, 17, and 18 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded on February 26, 2004 in the United States Patent and Trademark Office at Reel 015082, Frame 0407, and an assignment recorded on June 24, 2004 in the United States Patent and Trademark Office at Reel 015508, Frame 0967. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on February 26, 2004 with claims 1 through 20. Claims 1-3, 6-9, 12-16, 19, and 20 were cancelled in previous responses. Claims 4, 5, 10, 11, 17, and 18 are presently pending. Claims 4-5, 10-11 and 17-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. (United States Patent No. 6,493,770) and further in view of Adams et al. (United States Patent No. 5,987,568).

Claims 5, 11, and 18 are being appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 5 is directed to an integrated controller (FIG. 2: 300; FIG. 3) for use in a peripheral device (FIG. 2: 250) for controlling high speed communications between a host computer (FIG. 2: 210) and the peripheral device (FIG. 2: 250) (page 2, line 21, to page 3, line 6), comprising:

a processor integrated with the controller (FIG. 2: 300; FIG. 3) for controlling communications on a bus using one or more communication functions (page 2, line 21, to page 3, line 6), wherein the processor performs at least one function for the peripheral device (FIG. 2: 250) in addition to the one or more communication functions, wherein the processor provides processing capacity for use by the peripheral device (FIG. 2: 250), and wherein the high speed communications conform to a USB standard (page 3, lines 7-29).

Independent claim 11 is directed to a method performed by a controller (FIG. 2: 300; FIG. 3) on a peripheral device (FIG. 2: 250) for controlling communications between a host computer (FIG. 2: 210) and the peripheral device (FIG. 2: 250) (page 2, line 21, to page 3, line 6), comprising the step of:

executing one or more communication functions that control communications on a bus using a first processor (FIG. 2: 280), wherein the first processor also performs at least one function for the peripheral device (FIG. 2: 250) in addition to the one or more communication functions (page 3, lines 7-29), wherein the processor (FIG. 2: 280) is integrated with the

controller (FIG. 2: 300; FIG. 3) (page 3, lines 7-20) and provides processing capacity for use by the peripheral device (FIG. 2: 250), and wherein the high speed communications conform to a USB standard (page 3, lines 21-29).

Independent claim 18 is directed to an integrated circuit for use in a peripheral device (FIG. 2: 250) (page 2, line 21, to page 3, line 6; page 5, line 21, to page 6, line 9), comprising:

a controller (FIG. 2: 300; FIG. 3) for high speed communications between a host computer (FIG. 2: 210) and at least one peripheral device (FIG. 2: 250), comprising:

a processor (FIG. 2: 280) integrated with the controller (FIG. 2: 300; FIG. 3) for controlling communications on a bus using one or more communication functions (page 3, lines 7-20), wherein the processor (FIG. 2: 280) performs at least one function for the peripheral device (FIG. 2: 250) in addition to the one or more communication functions, wherein the processor (FIG. 2: 280) provides processing capacity for use by the peripheral device (FIG. 2: 250), and wherein the high speed communications conform to a USB standard (page 3, lines 7-29).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 4-5, 10-11 and 17-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. and further in view of Adams et al.

ARGUMENT

Independent Claims 5, 11 and 18

Independent claims 5, 11, and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. and further in view of Adams et al. With regard to claims 5, 11, and 18, the Examiner asserts that Sartore teaches an integrated controller for use in a peripheral device for controlling high speed communications (citing element 71, FIG. 2) between a host computer (element 52, FIG. 2) and said peripheral device (element 54, FIG. 2), comprising: a processor (element 72, FIG. 2) integrated with said controller for controlling communications on a bus using one or more communication functions (col. 5, lines 18-23), wherein said processor

performs at least one function for said peripheral device in addition to said one or more communication functions (col. 5, lines 25-35).

The Examiner acknowledges that Sartore does not provide details on functions of the peripheral. The Examiner alleges that it would be inherent that the CPU controls at least one function of the peripheral device. The Examiner asserts that Adams teaches a single processor in a peripheral performing functions of the peripheral device.

As discussed hereinafter, the CPU 72 in the peripheral 54 of Sartore does not "perform at least one function for said peripheral device *in addition to* said one or more communication functions," as required by the independent claims. Rather, it is clear that the CPU 72 in Sartore is only used to *reconfigure* the peripheral over a USB interface 71. The CPU 72 is not used for the normal operation of the peripheral.

As indicated in the Abstract of Sartore (emphasis added):

> A system and method for *reconfiguring* a peripheral device connected by a computer bus and port to a host from a *first* generic configuration to a *second* manufacturer specific configuration is provided in which the configuration of a peripheral device may be electronically reset. A peripheral interface device for a standardized computer peripheral device bus and port is also provided in which a physical disconnection and reconnection of the peripheral device is *emulated to reconfigure* the bus and port for a particular peripheral device.

See, also, col. 5, lines 23-25, where it is noted that memory 74 may initially contain an identification code to indicate which *configuration information* set should be *downloaded* to the peripheral device.

Thus, among other limitations, the CPU 72 of Sartore does not disclose or suggest performing at least one function for said peripheral device *in addition to* said one or more communication functions, or *provide* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

Adams is cited for a processor in a peripheral for performing and controlling functions of the peripheral. Adams does *not* disclose or suggest a processor *integrated with said controller* for performing at least one function for said peripheral device *in addition to* said one or more communication functions, or *provide* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

In the Response to Arguments section of the final Office Action, the Examiner acknowledges that Sartore is primarily focused on the disclosure with respect to reconfiguring the peripheral device, but asserts that it would be hard to argue that processors for peripheral devices would not be configured to perform at least one function for said peripheral device. The Examiner further asserts that it is widely accepted that, unless specifically stated that the processor of the host computer relieves the peripheral processor of processing capacity, one can confidently assume that the cited processor of peripheral devices is configured to perform functions for the peripheral devices.

Appellants maintain that the cited prior art does *not* disclose or suggest that a processor *integrated with said controller* for performing at least one function for said peripheral device *in addition to* said one or more communication functions. Moreover, the Examiner has provided *no* evidence to support an assertion that "it is widely accepted that, unless specifically stated that the processor of the host computer relieves the peripheral processor of processing capacity, one can confidently assume that the cited processor of peripheral devices are configured to perform functions for the peripheral devices." Appellants note that, were such a statement widely known, there would exist prior art disclosing such a feature.

Thus, Appellants respectfully request that the rejection of the cited claims under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. and further in view of Adams et al. be withdrawn.

Conclusion

The rejections of the cited claims under section 103 in view of Sartore et al. and Adams et al., alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

Date: June 28, 2010

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CLAIMS APPENDIX

1. (Cancelled).

2. (Cancelled).

3. (Cancelled).

4. The controller of claim 5, wherein said at least one peripheral device employs said processor to perform each of said functions of said at least one peripheral device.

5. An integrated controller for use in a peripheral device for controlling high speed communications between a host computer and said peripheral device, comprising:

a processor integrated with said controller for controlling communications on a bus using one or more communication functions, wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions, wherein said processor provides processing capacity for use by said peripheral device, and wherein said high speed communications conform to a USB standard.

6. (Cancelled).

7. (Cancelled).

8. (Cancelled).

9. (Cancelled)

10. The method of claim 11, wherein said at least one peripheral device employs said first processor to perform each of said functions of said at least one peripheral device.

11. A method performed by a controller on a peripheral device for controlling communications between a host computer and said peripheral device, comprising the step of:

executing one or more communication functions that control communications on a bus using a first processor, wherein said first processor also performs at least one function for said peripheral device in addition to said one or more communication functions, wherein said processor is integrated with said controller and provides processing capacity for use by said peripheral device, and wherein said high speed communications conform to a USB standard.

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Cancelled).

16. (Cancelled)

17. The integrated circuit of claim 18, wherein said at least one peripheral device employs said processor to perform each of said functions of said at least one peripheral device.

18. An integrated circuit for use in a peripheral device, comprising:

a controller for high speed communications between a host computer and at least one peripheral device, comprising:

a processor integrated with said controller for controlling communications on a bus using one or more communication functions, wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions, wherein said processor provides processing capacity for use by said peripheral device, and wherein said high speed communications conform to a USB standard.

19. (Cancelled).

20. (Cancelled).

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EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.